General Description

The LB4310 is a monolithic IC specifically designed to regulate the output current and voltage levels of switching battery chargers and power supplies

The device contains two Op Amps and a 2.5V precision shunt voltage reference. Op Amp 1 is designed for voltage control with its non-inverting input internally connected to the output of the shunt regulator. Op Amp 2 is for current control with both inputs uncommitted. The IC offers the power converter designer a control solution that features increased precision with a corresponding reduction in system complexity and cost.

The LB4310 is available in SOP-8 package.

Features

Voltage Reference

- Fixed Output Voltage Reference: 2.5V
- Reference Voltage Tolerance :±0.4%
- Sink Current Capability: 0.05 to 80mA
- Typical Output Impedance: 0.2Ω

OP Amp

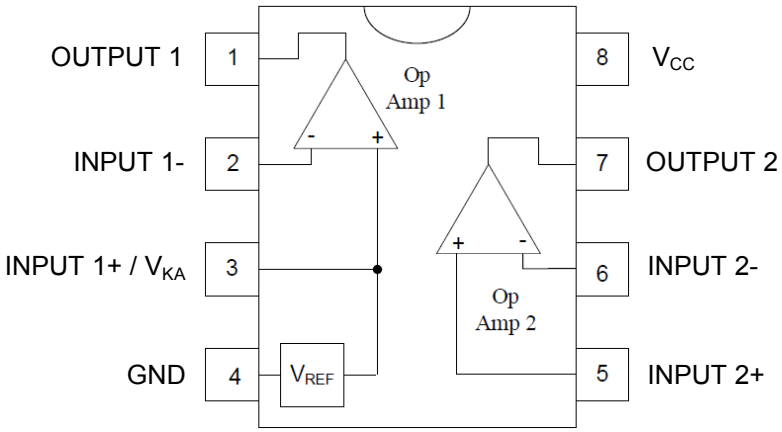
- Input Offset Voltage: 0.5mV
- Supply Current: 75μA per OP Amp at 5.0V Supply Voltage
- Unity Gain Bandwidth:1MHz
- Output Voltage Swing: 0 to V_{CC}-1.5V
- Power Supply Range: 3 to 36V

Applications

- Battery Charger
- Switching Power Supply

Please be aware that an **Important Notice** concerning availability, disclaimers, and use in critical applications of LSC products is at the end of this document.

Block Diagram



Ordering Information

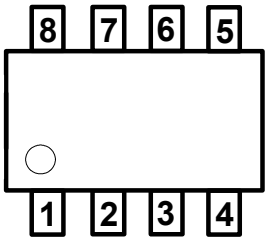
LB 4310 X XX X

- X → Pin-out Version
- XX → Package Type
- X → Pin Count

Pin-out Version	Package Type	Pin Count
A (SOP-8L) 1. OUTPUT 1 2. INPUT1- 3. INPUT1+ / V_{KA} 4. GND 5. INPUT2+ 6. INPUT2- 7. OUTPUT 2 8. V_{CC}	AP : SOP	G: 8

Pin Assignment

SOP-8L
Top View



LB4310AAPG

01. OUTPUT 1
02. INPUT1-
03. INPUT1+ / V_{KA}
04. GND
05. INPUT2+
06. INPUT2-
07. OUTPUT 2
08. V_{CC}

Absolute Maximum Ratings (Note1)

Operate over the "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to such conditions for extended time may still affect the reliability of the device.

Parameter		Symbol	Value	Unit
Supply Voltage		V_{CC}	40	V
Differential Input Voltage		V_{ID}	40	V
Input Voltage		V_{IN}	-0.3 to 40	V
Junction Temperature Range		T_J	150	°C
Storage Temperature Range		T_{STR}	-65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)		T_{Lead}	260	°C
Thermal Resistance (Note2) (Junction to Ambient)	SOP-8L	θ_{JA}	150	°C/W
Thermal Resistance (Junction to Case)	SOP-8L	θ_{Jc}	60	°C/W
Power Dissipation	SOP-8L	P_D	810	mW
ESD Withstand Voltage : -Human Body Model (HBM) -Machine Model (MM)		V_{ESD}	2000 200	V V
Moisture Sensitivity		MSL	Please refer the MSL label on the IC package bag/carton for detail	

Note1. Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note2. Thermal Resistance (Junction to Ambient) is measured at T_A = 25°C on a low effective thermal conductivity test board.

Recommended Operating Conditions (Note3)

Characteristics	Min	Max	Unit
Supply Voltage,V_{CC}	3	36	V
Operating Ambient Temperature Range, T_A	-40	105	°C

Note3. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{CC}=5V, GND=0V, T_A=25°C, unless otherwise specified.)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Units
Total Supply Current, excluding Current in Voltage Reference		I_{total}	V_{CC}=5V, no load, T_A=-40°C~105°C		-	0.15	0.25	mA
			V_{CC}=30V, no load, T_A=-40°C~105°C		-	0.20	0.30	
Voltage Reference Section								
Reference Voltage		V_{REF}	I_{KA} = 10mA	T_A=25°C	2.490	2.500	2.510	V
				T_A=-40°C~105°C	2.480	2.500	2.520	
Deviation of Reference Input Voltage over full temperature Range		$V_{REF(DEV)}$	I_{KA} = 10mA, T_A=-40°C~105°C		-	5	24	mV
Minimum Cathode Current for Regulation		$I_{KA(min)}$			-	0.01	0.05	mA
Dynamic Output Impedance		Z_{KA}	I_{KA} = 1 to 80mA, Frequency ≤ 1KHz		-	0.2	0.5	Ω
Op Amp 1 Section (VCC = 5V, VO = 1.4V, TA = +25°C, unless otherwise noted.)								
Input Offset Voltage		V_{IO}	T_A=25°C		-	0.5	3	mV
			T_A=-40°C~105°C		-	-	5	
Input Offset Voltage Temperature Drift		$V_{IO(TD)}$	T_A=-40°C~105°C		-	9	-	μV/°C
Input Offset Current		I_{IO}	T_A=25°C		-	2	30	nA
Input Bias Current		I_{BIAS}	T_A=25°C		-	20	150	nA
Large Signal Voltage Gain		G_V	V_{CC} = 15V, R_L = 2kΩ,V_O = 1.4V to 11.4V		85	100	-	dB
Power Supply Rejection Ratio		PSRR	V_{CC} = 5V to 30V		70	90	-	dB
Output Current	Source	I_{SOURCE}	V_{CC} = 15V, V_{ID} = 1V, VO = 2V		20	40	–	mA
	Sink	I_{SINK}	V_{CC} = 15V, V_{ID} = -1V, VO = 2V		5	20	–	
Output Voltage Swing		V_{OH}	V_{CC} = 30V, R_L = 10kΩ, V_{ID} = 1V		27	28	–	V
		V_{OL}	V_{CC} = 30V, R_L = 10kΩ, V_{ID} = -1V		-	100	150	mV

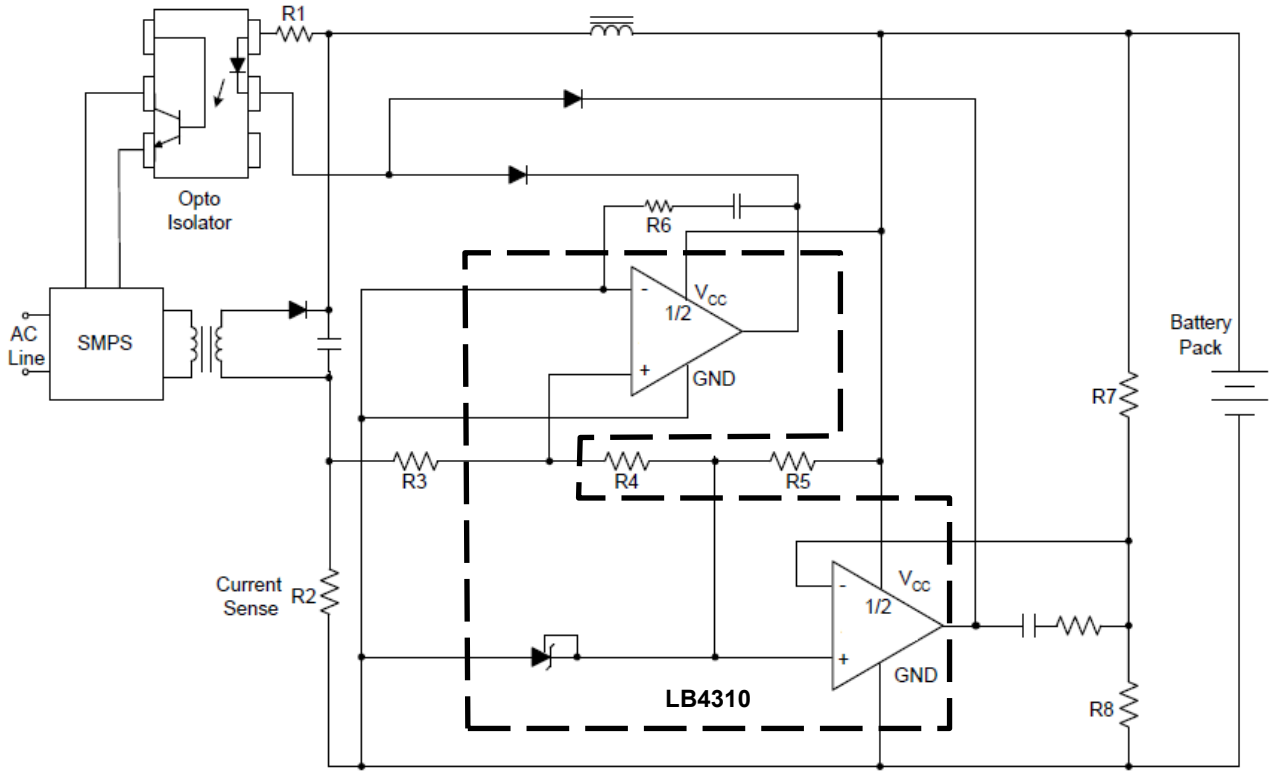
Electrical Characteristics(Cont.)

(V_{CC}=5V, GND=0V, T_A=25°C, unless otherwise specified.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Slew Rate		SR	V_{CC} = 18V, R_L = 2kΩ, AV = 1, V_{IN} = 0.5V to 2V, C_L = 100pF	0.2	0.5	–	V/μs
Unity Gain Bandwidth		U_{GBW}	V_{CC} = 30V, RL = 2kΩ, C_L = 100pF	0.7	1.0	–	MHz
Op Amp 2 Section (VCC = 5V, VO = 1.4V, TA = +25°C, unless otherwise noted.)							
Input Offset Voltage		V_{IO}	T_A=25°C	-	0.5	3	mV
			T_A=-40°C~105°C	-	-	5	
Input Offset Voltage Temperature Drift		$V_{IO(TD)}$	T_A=-40°C~105°C	-	9	-	μV/°C
Input Offset Current		I_{IO}	T_A=25°C	-	2	30	nA
Input Bias Current		I_{BIAS}	T_A=25°C	-	20	150	nA
Large Signal Voltage Gain		G_V	V_{CC} = 15V, R_L = 2kΩ,V_O = 1.4V to 11.4V	85	100	-	dB
Power Supply Rejection Ratio		PSRR	V_{CC} = 5V to 30V	70	90	-	dB
Output Current	Source	I_{SOURCE}	V_{CC} = 15V, V_{ID} = 1V, VO = 2V	20	40	–	mA
	Sink	I_{SINK}	V_{CC} = 15V, V_{ID} = -1V, VO = 2V	5	20	–	
Output Voltage Swing		V_{OH}	V_{CC} = 30V, R_L = 10kΩ, V_{ID} = 1V	27	28	–	V
		V_{OL}	V_{CC} = 30V, R_L = 10kΩ, V_{ID} = -1V	-	100	150	mV
Slew Rate		SR	V_{CC} = 18V, R_L = 2kΩ, AV = 1, V_{IN} = 0.5V to 2V, C_L = 100pF	0.2	0.5	–	V/μs
Unity Gain Bandwidth		U_{GBW}	V_{CC} = 30V, RL = 2kΩ, C_L = 100pF	0.7	1.0	–	MHz

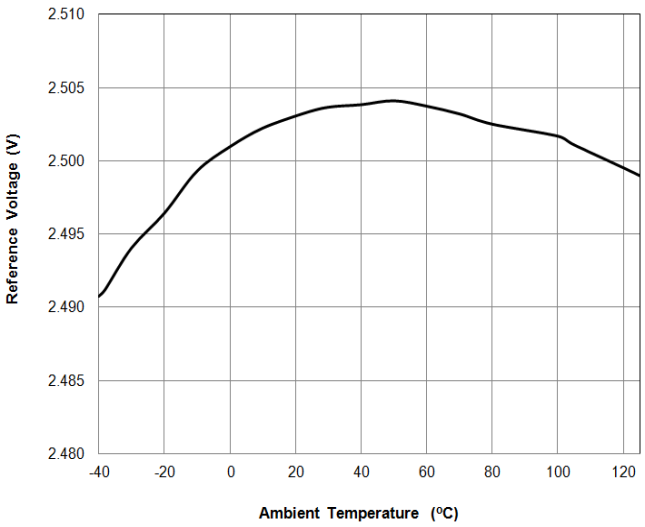
Note 4: The full temperature characteristics are guaranteed by design. They are not tested in production.

Application Circuit

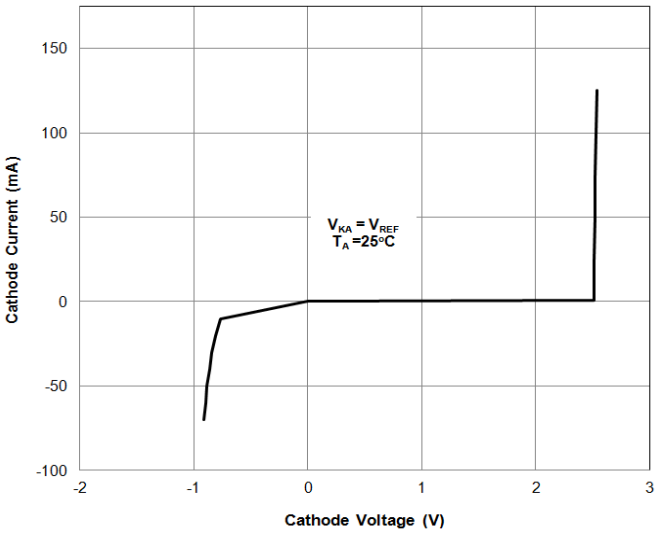


Typical Characteristics

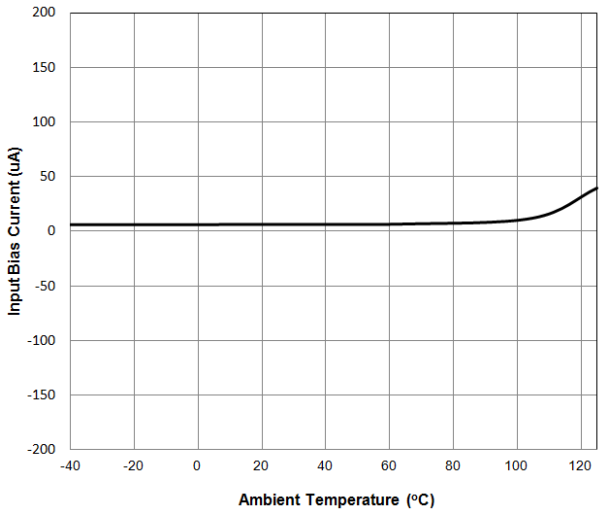
Reference Voltage vs. Ambient Temperature



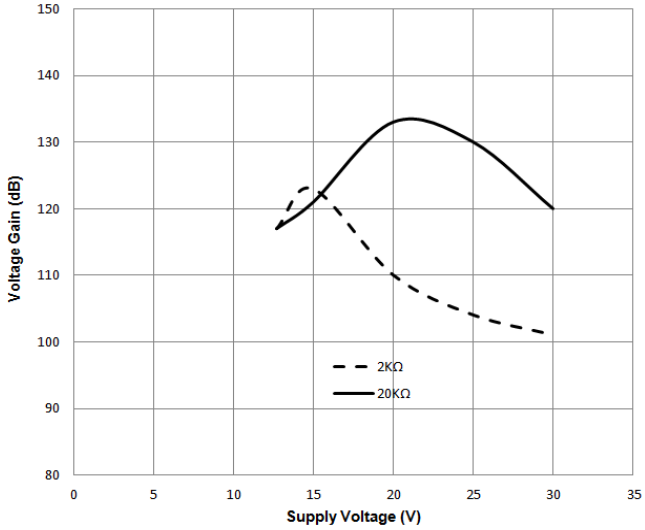
Cathode Current vs. Cathode Voltage



Input Bias Current vs. Ambient Temperature

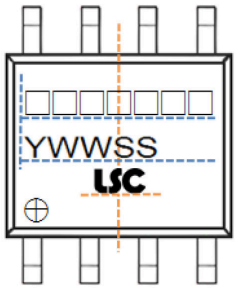


Op Amp Voltage Gain



Marking Information

SOP-8L

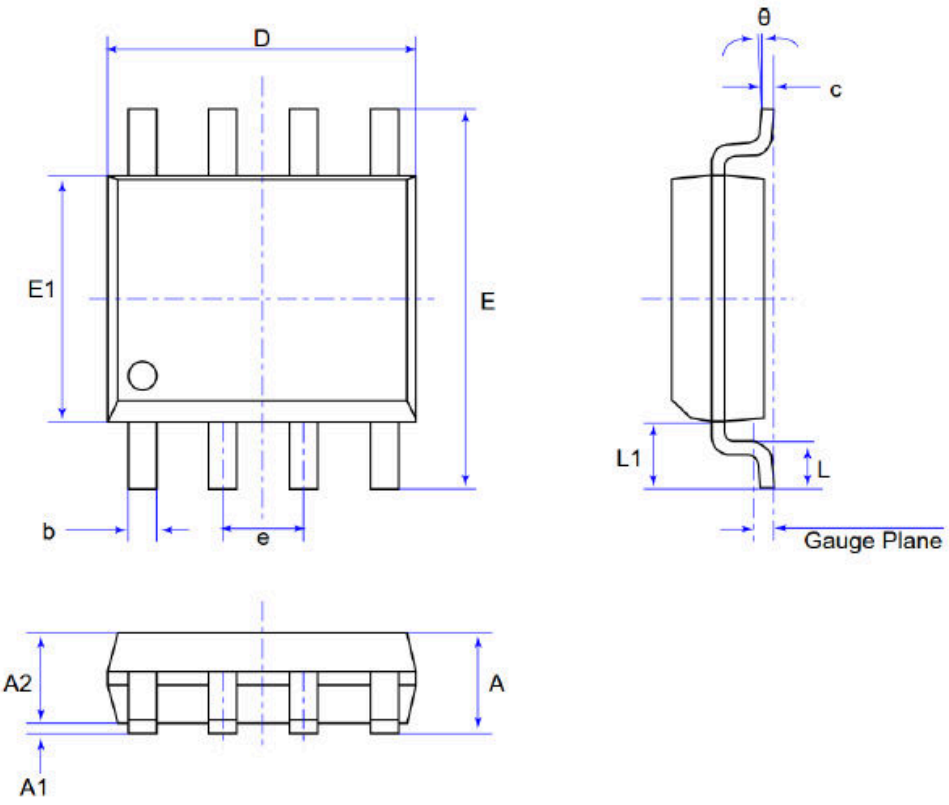


1) □□□□□□□= Marking Name
B4310P = LB4310AAPG

2) YWWSS = Date Code
Y = Year
WW = Week
SS = Internal Code

Mechanical Information

SOP-8L



Unit : mm

Symbol	Min	Max
A	-	1.75
A1	0.10	0.25
A2	1.25	1.65
b	0.33	0.51
c	0.10	0.26
D	4.70	5.10
E	5.80	6.20
E1	3.70	4.10
e	1.27 REF	
L	0.40	1.27
L1	1.04 REF	
Gauge Plane	0.25 BSC	
θ	0°	8°

MSL (Moisture Sensitive Level) Information

IPC/JEDEC J-STD-020D.1 Moisture Sensitivity Levels Table

LEVEL	FLOOR LIFE		SOAK REQUIREMENTS				
			Standard		Accelerated Equivalent [1]		
					eV 0.40-0.48	eV 0.30-0.39	CONDITION
	TIME	CONDITION	TIME (hours)	CONDITION	TIME (hours)	TIME (hours)	
1	Unlimited	≤30 °C /85% RH	168 +5/-0	85 °C /85% RH	NA	NA	NA
2	1 year	≤30 °C /60% RH	168 +5/-0	85 °C /60% RH	NA	NA	NA
2a	4 weeks	≤30 °C /60% RH	696[2] +5/-0	30 °C /60% RH	120 -1/+0	168 -1/+0	60 °C/ 60% RH
3	168 hours	≤30 °C /60% RH	192[2] +5/-0	30 °C /60% RH	40 -1/+0	52 -1/+0	60 °C/ 60% RH
4	72 hours	≤30 °C /60% RH	96[2] +2/-0	30 °C /60% RH	20 +0.5/-0	24 +0.5/-0	60 °C/ 60% RH
5	48 hours	≤30 °C /60% RH	72[2] +2/-0	30 °C /60% RH	15 +0.5/-0	20 +0.5/-0	60 °C/ 60% RH
a	24 hours	≤30 °C /60% RH	48[2] +2/-0	30 °C /60% RH	10 +0.5/-0	13 +0.5/-0	60 °C/ 60% RH
6	Time on Label (TOL)	≤30 °C /60% RH	TOL	30 °C /60% RH	NA	NA	NA

Note 1: CAUTION - To use the ‘‘accelerated equivalent’’ soak conditions, correlation of damage response (including electrical, after soak and reflow), should be established with the ‘‘standard’’ soak conditions. Alternatively, if the known activation energy for moisture diffusion of the package materials is in the range of 0.40 - 0.48 eV or 0.30 - 0.39 eV, the ‘‘accelerated equivalent’’ may be used. Accelerated soak times may vary due to material properties (e.g .mold compound, encapsulant, etc.). JEDEC document JESD22-A120 provides a method for determining the diffusion coefficient.

Note 2: The standard soak time includes a default value of 24 hours for semiconductor manufacturer’s exposure time (MET) between bake and bag and includes the maximum time allowed out of the bag at the distributor’s facility. If the actual MET is less than 24 hours the soak time may be reduced. For soak conditions of 30 °C/60% RH, the soak time is reduced by 1 hour for each hour the MET is less than 24 hours. For soak conditions of 60 °C/60% RH, the soak time is reduced by 1 hour for each 5 hours the MET is less than 24 hours. If the actual MET is greater than 24 hours the soak time must be increased. If soak conditions are 30 °C/60% RH, the soak time is increased 1 hour for each hour that the actual MET exceeds 24 hours. If soak conditions are 60 °C/60% RH, the soak time is increased 1 hour for each 5 hours that the actual MET exceeds 24 hours.